Low-Distortion MMIC Power Amplifier Using a New Form of Derivative Superposition

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***Abstract*—Reduction of interchannel interference produced by a power amplifier near 1-dB compression is a key concern for the wireless communications industry. In this paper, we present a 100-mW monolithic-microwave integrated-circuit (MMIC) power amplifier designed using a novel form of the derivative superposition method. The measured results of the MMIC power amplifier showed a two-tone carrier-to-interference (C/I) ratio of 45 dBc with an efficiency of 22.5% when backed off by 4.5 dB from the 1-dB compression point. We demonstrate that the MMIC power amplifier represents a good compromise between C/I ratio, output power, efficiency, and gain at the cost of an increase in total gate width, by comparing it to class-A, class-AB, and class-B single field-effect-transistor amplifiers.**

***Index Terms*—Intermodulation distortion, MMIC power amplifiers.**

I. Introduction

IN MODERN multichannel high-capacity wireless communication systems, there is a stringent requirement to minimize interference to adjacent channels to prevent data loss. This is a particular concern in power amplifiers where operation close to 1-dB compression is highly desirable. A number of practical system-level black-box techniques have been proposed for reducing adjacent channel interference arising from nonlinear device behavior including predistortion, feedforward, and Cartesian loop feedback. An alternative approach is to minimize distortion at a circuit level. One such approach is the derivative superposition (DS) method [1], [2]. This utilizes several parallel FETs of different gate width and gate bias to alter the nonlinear behavior of a main FET. The key difficulty with extending such techniques to large signals is that available computer-aided design (CAD) models do not correctly describe large-signal frequency dispersion effects seen in GaAs FETs [3], [4], which critically affect the accuracy of third-order intermodulation distortion (IMD3) simulations. Typical accuracy of intermodulation distortion simulation in the presence of significant bias-dependent frequency dispersion is shown in [5]. In multiFET circuits, measurement-based design approaches (such as [2] and [6]) are useful for minimizing small-signal distortion, but are very difficult to modify for minimizing large-signal distortion. Another multiFET approach is the Doherty amplifier [7], which obtains high efficiency for a range of modulation levels by using two FETs at different bias points.

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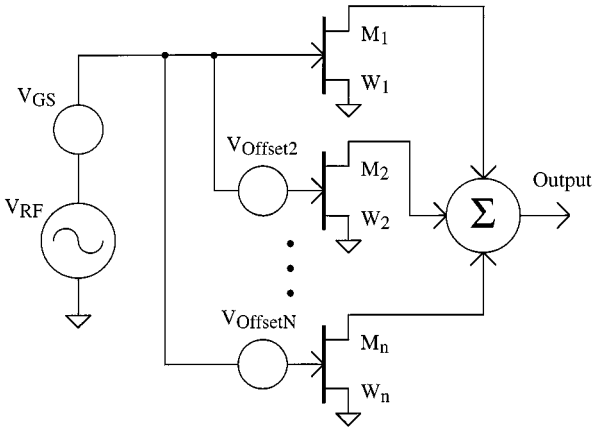

Fig. 1. Idealized schematic of a DS amplifier.

In this paper, we describe a new form of the DS technique that leads to high carrier-to-interference (C/I) ratio performance close to 1-dB compression and is sufficiently robust that it can be designed with existing CAD tools.

II. Technique

DS is the summation (and occasionally subtraction) of the derivatives of FET drain current (with respect to gate–source voltage) to achieve a desired transfer characteristic. This can be achieved by the parallel connection of several common-source FETs (M_1–M_n) of different gate widths (W_1–W_n) and gate bias points with ac coupled gates, as shown in Fig. 1. Usually, the summation of drain currents can be achieved by direct connection of the drains to the output. In [2], the authors previously designed the circuit to have low small-signal IMD3 at the quiescent point to minimize IMD3 for a range of signal amplitudes. This was achieved by reducing the magnitude of the third derivative of drain current with respect to gate–source voltage (the g_3 derivative) at the quiescent point.

An alternative approach proposed here is to design the circuit not to reduce the magnitude of the g_3 derivative at the quiescent point, but to introduce a region of opposite sign around the quiescent point, as shown in Fig. 2(a). To understand its operation, it is necessary to use the concept of a time-dependent derivative, which was previously used to apply Volterra analysis to mixers in [8] and [9]. Under small-signal excitation, the g_3 derivative is essentially time invariant and finite, as shown in Fig. 2(b). As the level of excitation is increased, the peaks of the signal pass into the two adjoining regions where the g_3 derivative has an opposite sign. This results in a time-varying g_3 derivative, shown in Fig. 2(c). For large signals, the signal will spend much

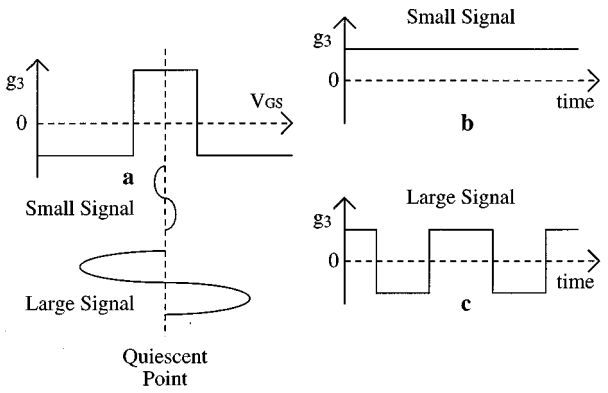

Fig. 2. (a) Idealized variation of the third derivative of drain current (g_3) with gate–source voltage for the novel DS amplifier around its quiescent point. (b) Variation of g_3 with time under small-signal excitation. (c) Variation of g_3 with time under large-signal excitation.

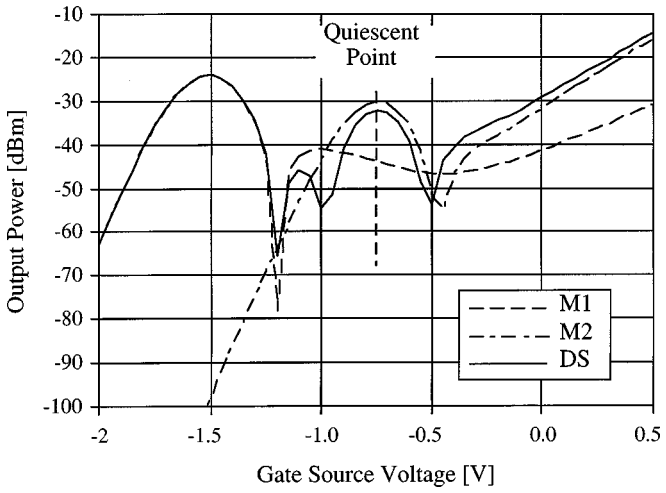

Fig. 3. Simulation of the variation of small-signal third-order distortion with gate bias arising from $M1$ and $M2$ in the DS amplifier. A region of sign reversal occurs in the g_3 derivative at the quiescent point ($V_{\rm GS} = -0.75$ V).

of the time in the surrounding regions of opposite sign, essentially reversing the polarity of the g_3 derivative. Depending on the waveform and g_3 derivative shape, there will exist an amplitude where the average of this time varying g_3 derivative is zero, leading to zero IMD3 at this signal amplitude.

In the case of the distortion nulling form of DS [2], it was necessary to determine the FET nonlinearity to a high degree of accuracy to obtain a working design. The sign reversal technique requires only a region of opposite sign to exist for correct operation. This can lead to a relaxation on the required CAD model accuracy, allowing working designs to be obtained with existing CAD models providing they describe the soft pinchoff behavior such as in [10] and [11]. These CAD models could not be used with the nulling technique of [2] with any confidence of success for frequency-dispersive FET technologies.

III. Design

A Parker–Skellern MESFET model [10] was extracted from dc and pulsed I–V measurements [12] for the Marconi Materials Technology F20 IG Implant process. The first stage of the design procedure was to design a class-A amplifier (M_1) that is to be linearized. For convenience, a nominal load of 50 Ω was chosen. A nominal drain bias ($V_{\rm DS}$) of 4.5 V was chosen to ensure that gate–drain breakdown would not occur under normal operation. To obtain approximately maximum possible output power, the load line should run from the middle of the knee region at maximum drain current and have zero current around $V_{\rm DS} = 8.5$ V. For a 50-Ω load, this requires a FET gate width of 6×100 μm, producing a nominal output power of 100 mW in 50 Ω. A nominal gate bias of -0.75 V was then chosen.

The second stage of the design process was to introduce a second FET (M_2) to this amplifier such that the positive peak in its g_3 derivative with gate bias is aligned with the quiescent point of M_1 (which is in the region where the g_3 derivative of M_1 is negative). The magnitude of the g_3 derivative of an FET is proportional to its gate width. The gate width of M_2 was chosen to ensure that the positive peak in g_3 of M_2 is greater than the negative g_3 derivative of M_1, thus generating a region of sign reversal at the quiescent point. In Fig. 3, we show the results of a Volterra analysis of the IMD3 of the DS circuit (together with the individual contributions arising from M_1 and M_2) with bias (with a constant offset in the gate–source voltage of M_2 relative to M_1). Although here, M_2 is larger than M_1, its g_3 peak appears smaller than that of M_1. This is due to the combined output conductance of M_1 and M_2 being significantly higher at the quiescent point than for the case at the g_3 peak of M_1. Each null in the IMD3 corresponds to a reversal in sign of the g_3 derivative.

The FETs were then width scaled so that the circuit had approximately the same small-signal gain as the original 6×100 μm class-A amplifier. The design process was carried out using an in-house software tool specifically written for designing DS circuits, although a nonlinear circuit simulator could have also been used. The design was then verified in SPICE3f4. It was noted that further increasing the gate width of the secondary device moved the distortion null to higher power levels. However, the improvement became asymptotic at gate widths greater than 2.5 times the reference device (M_1). In this design, it was decided to use a secondary device (M_2) of gate width 1.5 times that of the reference device to achieve a reasonable compromise between circuit performance and overall chip area. A schematic of the full design together with the intermodulation-distortion measurement test set is given in Fig. 4.

A photograph of the prototype MMIC design is shown in Fig. 5. The chip dimensions are 961 μm $\times$ 764 μm. To allow flexibility to test over a wide range of frequencies and bias conditions, no matching networks were used on the prototype monolithic microwave integrated circuit (MMIC). Instead, a 50-Ω resistor was used at the RF input port to provide a wide-band RF input termination. The RF input port (left-hand side) also provides the gate bias for $M1$. The gate of $M2$ is biased through a dc pad and ac coupled to the RF input port through an *RC* network. The RF output port (right-hand side) also provides dc drain bias for both FETs.

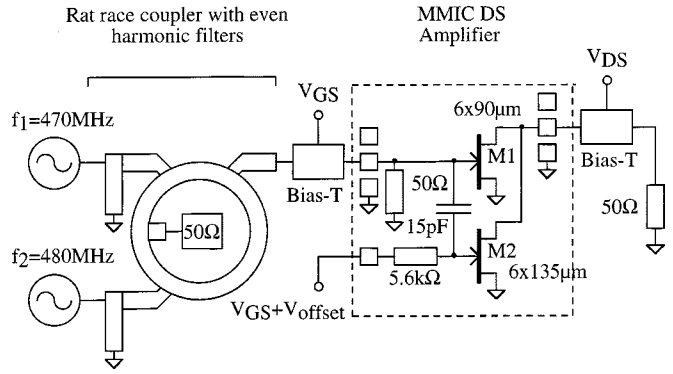

Fig. 4. Schematic diagram of the MMIC DS amplifier with two-tone test circuit and biasing.

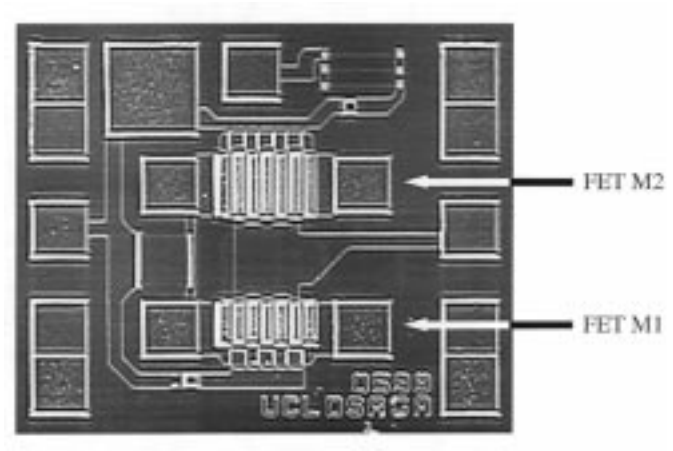

Fig. 5. Photograph of MMIC implementation of the DS amplifier.

IV. Measured Performance

In this section, we present measured results on the MMIC. Not only was it possible to measure the complete DS amplifier, but it was also possible to operate each FET individually, allowing comparisons with single FET amplifiers. The designs are defined in Table I. They include the DS amplifier working into a 50-Ω load, M_1 of the DS amplifier operating in class-A mode working into a 50-Ω load with M_2 turned off, and M_2 of the DS amplifier operating in class-B and class-AB modes working into a 50-Ω load with M_1 turned off.

The use of the same load resistor and drain bias for all designs means that the designs are not all fully optimized, but the results are considered to be representative.

Two-tone IMD3 measurements were made with two tones at 0.47 and 0.48 GHz, combined with a rat-race isolating coupler with $\lambda/4$ short-circuited coax stubs at the inputs of the coupler (to filter out even harmonics) to minimize residual distortion, as shown in Fig. 4. Test results at these frequencies are considered representative of circuit performance over a range of frequencies where the intrinsic device capacitances do not significantly affect performance. The relatively wide tone spacing of 10 MHz was chosen to minimize residual distortion generated in the spectrum analyzer.

The measured IMD3 plotted as C/I ratios with output power for the designs are presented in Fig. 6. It can be seen that the DS amplifier produces a strong peak at high output power in the C/I plot as expected. The class-A and class-B amplifiers did not produce any peaks in the C/I plot. The class-AB amplifiers have weak peaking effects in the C/I curves that vary strongly with gate bias.

TABLE I
Circuit Designs Tested and Their Output Refrrred 1-dB Compression Points ($P_{1\ \mathrm{dB}}$) and Efficiancies at their 1-dB Compression Points (η) (R_L = 50 Ω and V_{DS} = 4.5 V)

Class	DS	A	AB2	AB1	B
FETs*	M1+M2	M1	M2	M2	M2
V_{GS1}[V]	-0.75	-0.75	-	-	-
V_{GS2}[V]	-1.55	-	-1.0	-1.25	-1.55
P^{+}_{1dB}[dBm]	20.2	18.1	18.0	≈18.5	≈19.5
η^{+}[%]	47.3	37.5	39.5	≈42.0	≈43.5
$P^{\$}_{1dB}$[dBm]	14.6	13.1	11.6	≈11.0	≈9.5
$\eta^{\$}$[%]	68.1	43.4	26.6	≈28.0	≈31.0

* gate widths M1 = 540μm and M2 = 810μm

$^{+}$ 1 tone 0.48GHz; $^{\$}$ 2 tones 0.47 and 0.48GHz

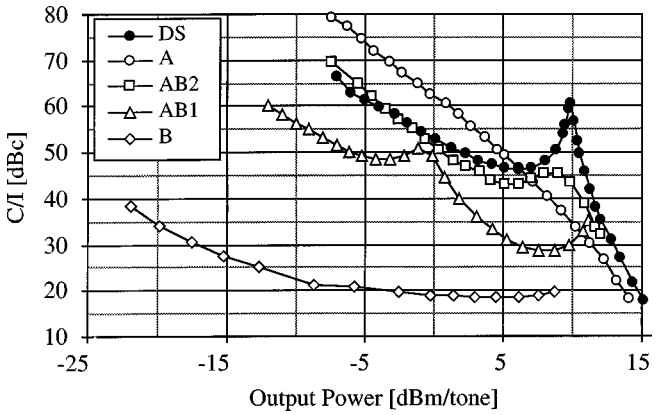

Fig. 6. Measured variation of two-tone C/I ratio with output power level for various types of amplifiers.

It was noted that the measured peak in C/I ratio for the DS amplifier occurred at an output power of 9.9 dBm, whereas in simulation, it occurred at an output power of 7.5 dBm. The measured 1-dB compression point was 0.6 dB higher than that simulated. These differences are attributed to a combination of process variation and weakness of the CAD model to accurately describe the large-signal nature of the frequency dispersion in the process.

Fig. 7 depicts contour graphs of the measured two-tone IMD3 plotted as C/I ratio (C/I) with gate bias and input power for the 540-μm single FET and DS amplifier (with a constant offset in the gate–source voltage of M_2 relative to M_1). It can be seen that, for the single FET amplifier in Fig. 7(a), a peak in C/I occurs at low-signal levels near the class-AB operating point. As the RF power is increased, this peak continues to exist, but moves to progressively higher gate bias voltages. This feature remains strongly bias dependent and, hence, relatively sensitive

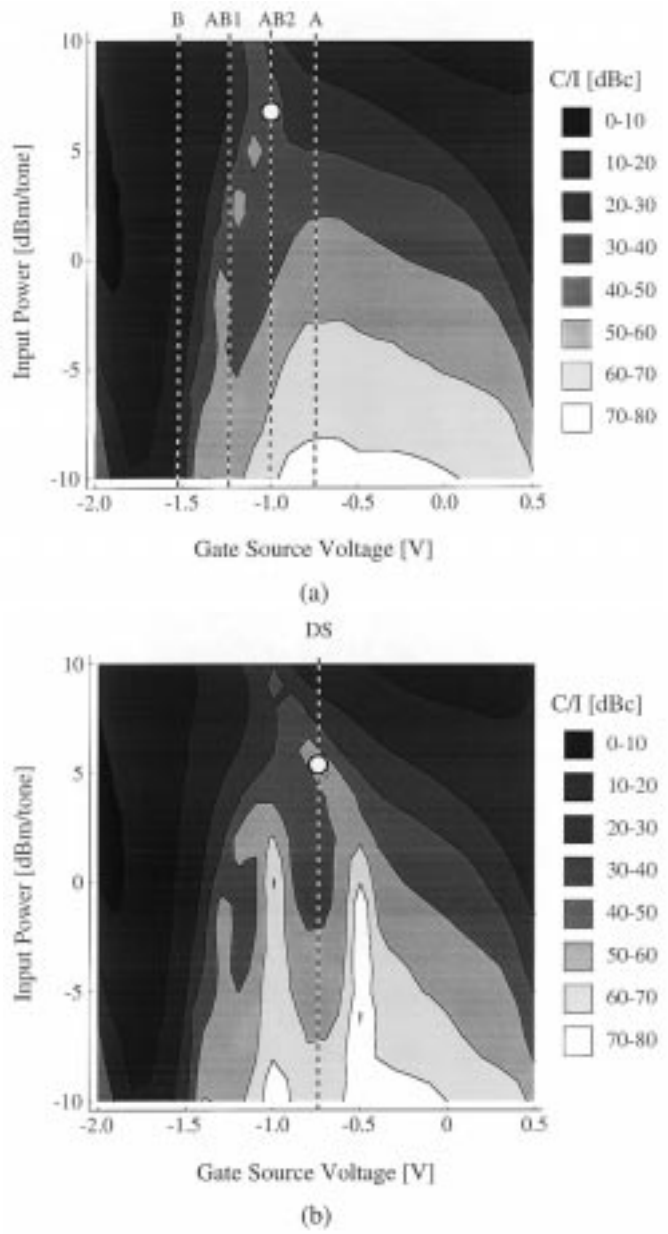

Fig. 7. Contour graphs of C/I with input power and gate source bias for: (a) class-A, class-AB1, class-AB2, and class-B amplifiers and (b) DS amplifier. Quiescent points indicated by dotted lines and C/I peaks indicated by circles. Two tones at 0.47 and 0.48 GHz.

to drift. In Fig. 7(b), we observe that two of the three C/I peaks, visible for the DS amplifier at low power, combine and cancel as the input power level increases. The remaining peak curves with respect to gate bias crossing through the quiescent point at high power, leading to the peak in C/I observed in Fig. 6. The relatively strong curvature with gate bias means that the feature is relatively insensitive to bias drift compared to the peak generated by the class-AB operating point.

In order to allow a better comparison of amplifier performance, the measured output referred 1-dB compression points (single- and two-tone) for the designs are presented in Table I. Due to the limitation of the test equipment and the shape of the curves for the class-B and class-AB1 amplifiers, their 1-dB compression points could not be determined precisely and approximate values were extrapolated. For the amplifiers exhibiting gain enhancement, we define 1 –dB compression as being 1 dB below the peak gain. Table I also summarizes the single- and two-tone efficiencies at 1-dB compression for each of the five amplifiers.

TABLE II
OUTPUT POWER (P_{out}), EFFICIENCY, GAIN, AND DEGREE OF BACKOFF FROM 1-dB COMPRESSION POINT (BO) TO MEET A TWO-TONE 45-dBc C/I RATIO

Class	P_{out}[dBm]	Efficiency[%]	gain[dB]	BO[dB]
DS	11	22.5	4.5	4.5
A	7	8.0	3.9	6.0
AB2	9	18.5	2.2	2.6
AB1	0.75	6.8	-1.0	≈10.2
B	-22	0.3	-10.8	≈31.5

To illustrate the potential advantage of the DS circuit, we consider a hypothetical example that requires a minimum two-tone C/I ratio of 45 dBc over a wide signal range. From Fig. 6, we have determined the maximum output power for which the amplifiers of Table I meet the 45 dBc C/I ratio requirement. For this condition, we have tabulated the output power (P_{out}), efficiency, gain, and degree of backoff from 1-dB compression point (BO) in Table II. It can be seen that the DS amplifier has the highest output power, highest efficiency, and highest gain. The class-AB2 amplifier has the lowest backoff and good efficiency, but has a significantly lower gain, and in the light of the contour graphs of Fig. 7, is more sensitive to gate bias. The class-A amplifier has high gain and good output power, but poor efficiency. The class-AB1 and class-B amplifiers have output power and efficiency, under the requirement of a 45 dBc C/I ratio, which is too low to be directly useful.

V. CONCLUSIONS

A 100-mW MMIC power amplifier utilizing a novel form of DS, which has a region of sign reversal in its g_3 derivative around the quiescent point, has been described in this paper. The circuit can be designed with existing CAD models providing they describe soft pinchoff behavior. The MMIC DS power amplifier achieved a two-tone C/I ratio of 45 dBc and an efficiency of 22.5% when backed off by 4.5 dB from the 1-dB compression point around 0.5 GHz. It achieved a good compromise between C/I ratio, output power, gain, and efficiency at the cost of a higher chip area than its single FET counterparts.

Now that it has been demonstrated that it is possible to design this circuit with the current CAD models it is, therefore, possible to further improve the circuit performance through optimizing the device gate widths and gate bias. Further work will also be directed toward determining the maximum frequency of the technique.

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